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Design and Implementation of Low Power 3-Bit Flash ADC Using 180nm CMOS Technology

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ABSTRACT
Analog-to-digital converter has become a very important device in today's digitized world as they have a very wide variety of applications. Among all the ADC's available, the Flash ADC is the fastest one but a main disadvantage of Flash ADC is its power consumption. So, this paper aims at implementing a low power high speed Flash ADC. A 3-bit Flash ADC has been designed using CMOS technology. A two stage open loop comparator and a priority encoder have been implemented using which the ADC has been designed. All the circuits are simulated using 180nm technology in Tanner EDA environment. The supply voltage Vdd is 1.8v.Analog output of each comparator depending upon the comparison between the input and the reference voltage is fed to the encoder and finally the compressed digital output is obtained. The power dissipation of each circuit implemented is calculated individually including other parameters like are, resolution gain and speed.
Keywords:Flash ADC, Comparator, Encoder, OR gate, Tanner EDA, CMOS Technology.

I. INTRODUCTION

Analog-to-digital converters (ADC's) are the most distinguished signal circuits which interface the world analog signals, the digital signal processing and computing world. ADC's includes three essential parameters which cannot be changed once it has been designed and the parameters are resolution, speed and power consumption.

ADC which is being designed these days needs an architecture having high speed of operation and less power consumption. One single ADC type cannot cover all applications since the performance parameters like sampling rate, power consumption and resolution of an ADC is basically determined by its architecture. Therefore, it is very important to choose an ADC for each particular application. Different type of ADC's are available like SAR ADC, Dual Slope ADC, Sigma Delta ADC and Flash ADC but among all the se the most commonly used ADC is The Flash adc because of its better tradeoff between its performance metrics. Flash ADC is mainly used for applications which require high speed and low resolution. Flash ADC architectures have been widely studied because of its fast performance among all the ADC's available. It is faster due to its parallel architecture and hence it is also known as parallel ADC.

II. BASIC BUILDING BLOCKS:

A) COMPARATOR

The comparator is a circuit which compares one analog signal with another analog signal or a reference signal and produces binary signal as the output based on the comparison. Comparators are also known as 1-bit analog-to-digital converter. Fig. 1 shows symbol of comparator.

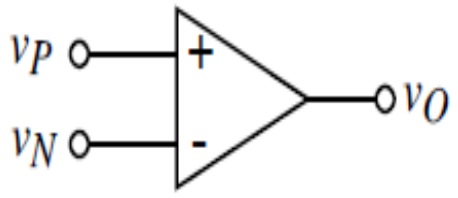

Fig. 1- Symbol of a Comparator

In Analog-to-Digital converters (ADC), comparators play an important role. The performance of the target application is significantly influenced by the type and architecture of the comparator. The comparator's input offset voltage, the delay and input signal range directly affects the speed and resolution of an ADC. Some basic applications of comparators are analog-to-digital conversion, signal detection, neural networks and function generation etc.

TWO STAGE OPEN LOOP COMPARATOR

Two stage open loop comparator circuits consist of two differential inputs. This comparator consists of input stage, differential amplifier and output stage as shown in Fig. 2. One of the advantages of this circuit is that the circuit consumes minimum number of transistor and thus the circuit area is small.

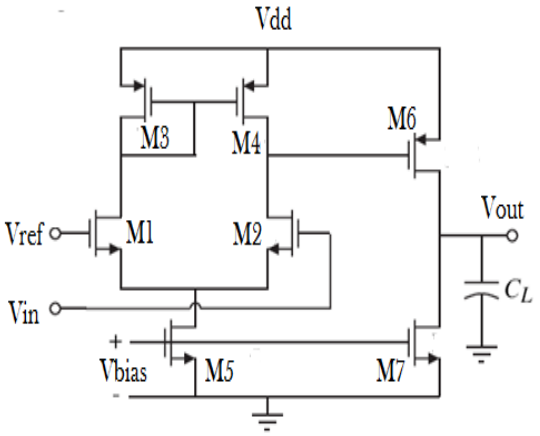

Fig -2: Two stage CMOS open loop comparator

Table 1:**Design Specification for comparator**

Technology	180nm CMOS Technology
Supply Voltage	1.8V
Slew Rate	8 V/µs
C_L	5pF
V_{out} Range	2.0V
Response Time	2.72ns

The two-stage op amp without compensation is an excellent implementation of a high-gain, open-loop comparator. In order to achieve the desired resolution Comparator requires differential input and sufficient gain. So, two stage op-amps make an excellent implementation of the comparator. Hence a simplification occurs because it is not necessary to compensate the comparator as it will generally be used in an open loop mode. In fact, it is preferred not to compensate the comparator so that it has the large bandwidth possible, which will give a faster response.

B) PRIORITY ENCODER

A priority encoder can be defined as a circuit that compresses multiple binary inputs into a smaller number of outputs and produces an output which is the binary representation of the original number starting from zero of the most significant input bit. By acting on the highest priority encoder they are often used to control interrupt requests. If two or more inputs are given at the same time to the encoder, the input having the highest priority takes the lead. Different types of priority encoders include 4 to 2, 8 to 3 priority encoders. The following fig. shows the truth table of 8 to 3 priority encoder.

Table 2: Truth Table of 8 to 3 priority encoder

Inputs								Outputs		
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y_2	Y_1	Y_0
1	0	0	0	0	0	0	0	0	0	0
x	1	0	0	0	0	0	0	0	0	1
x	x	1	0	0	0	0	0	0	1	0
x	x	x	1	0	0	0	0	0	1	1
x	x	x	x	1	0	0	0	1	0	0
x	x	x	x	x	1	0	0	1	0	1
x	x	x	x	x	x	1	0	1	1	0
x	x	x	x	x	x	x	1	1	1	1

III)FLASH ADC ARCHITECTURE

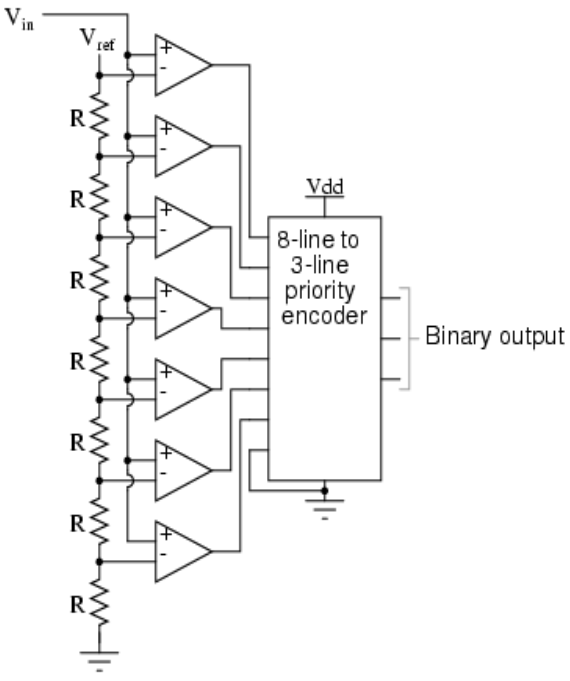

Fig 3: Circuit of 3-bit Flash ADC

Figure 3. Represents the circuit diagram of a 3 bit Flash ADC. Flash ADC requires 2N-1 number of comparators, 2N resistors and encoder for N bit resolution. For e.g. For a Flash Adc of 4-bit, we require 15 comparators and 8 resistors.An analog signal is fed to each voltage comparator to compare input voltage to reference voltages. Reference voltage is generated by the resistive

ladder circuit and depending on the comparison made between Vin and Vref, the comparator produces an output 0 or 1. If VIN is greater than Vref, the output is 1 otherwise 0. The compared analog input which means the output of the comparator is then fed to the priority encoder to get the digitized output. To reach at VDD R1 & R8 is taken as 2 Kohm whether others are 1Kohm. . Thus, comparator and encoder are the basic building block of a flash ADC.

(Iv) Implementationsand Results

1. Two Stage Open Loop Comparator (In Tanner Eda Using 180nm Technology)

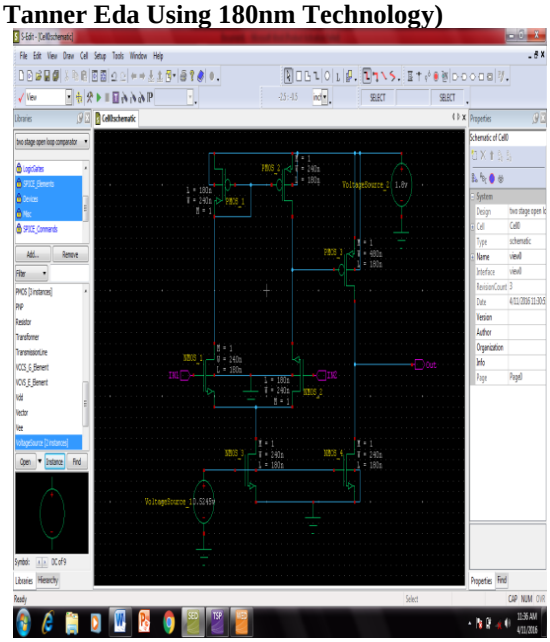

Fig. 4- Two stage open loop comparator

1.1 Transient Analysis

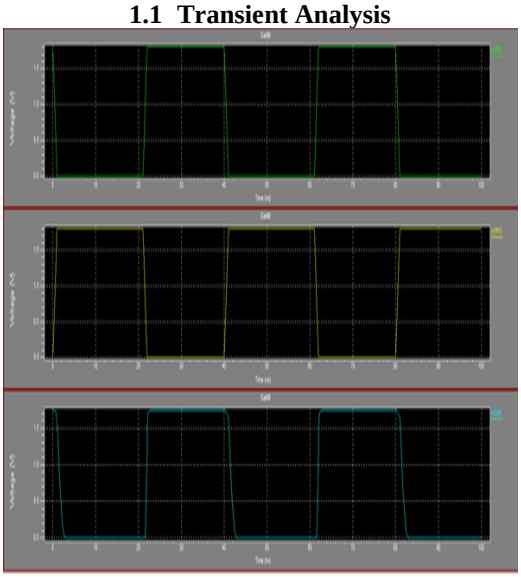

Fig. 5- Transient analysis of two stage comparator

1.2 AC Analysis

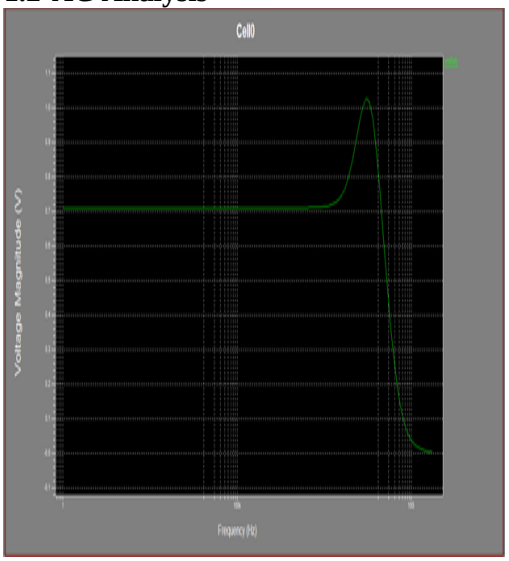

Fig. 6AC analysis of two stage open loopcomparator

3db frequency- 339.36 Hz

1.3 Power Result (open loop comparator)

VVoltageSource_2 from time 1e-008 to 1e-007
Average power consumed -> 2.370059e-005 watts
Max power 7.570612e-005 at time 4.1e-008
Min power 5.441084e-006 at time 2.1375e-008

2. Implementation Of 8x3 Priority Encoder (In Tanner Eda)

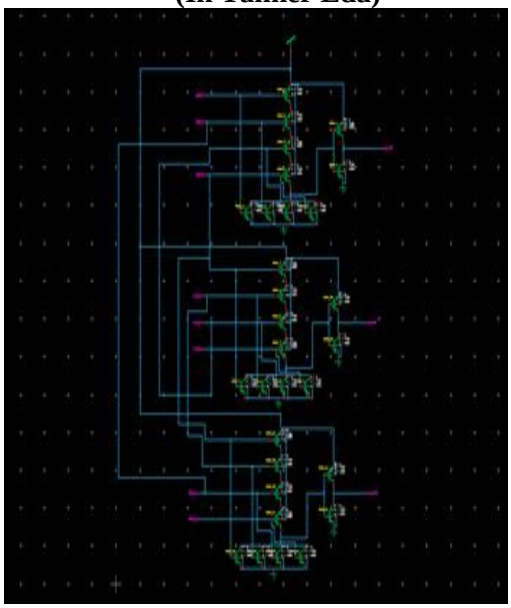

Fig. 7: 8x3 priority encoder using 4 input OR gates

2.1 Output Waveforms:

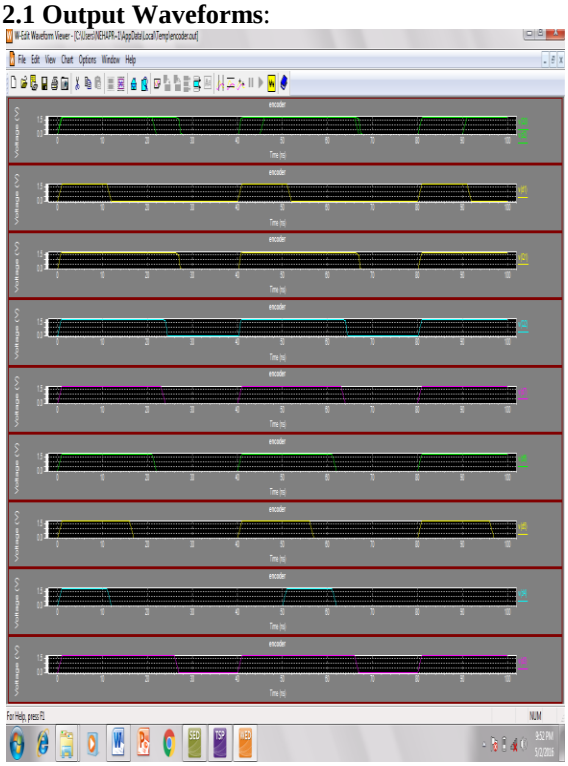

Fig 8: Output waveform of Priority Encoder

2.2 Power Results:

Vdd from time 1e-008 to 1e-007
Average power consumed -> 1.059128e-005 watts
Max power 2.593029e-004 at time 4.07411e-008
Min power 2.019536e-009 at time 5e-008

3. Implementation Of 4 Inputs Orgate

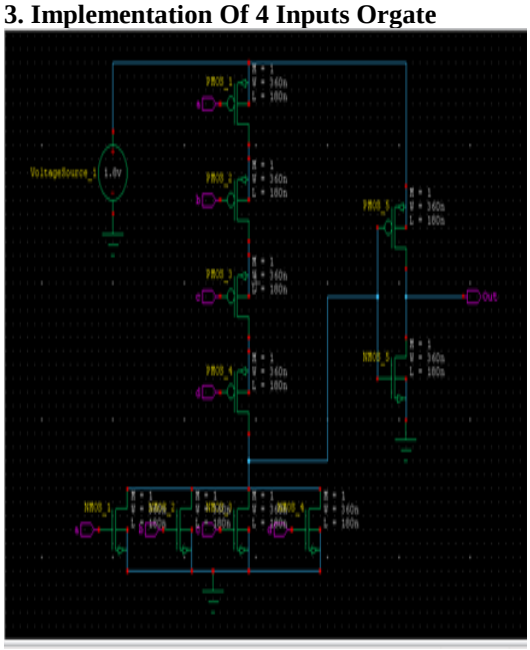

Fig 9: Schematic of 4 input OR gate

3.1 Output Waveform:

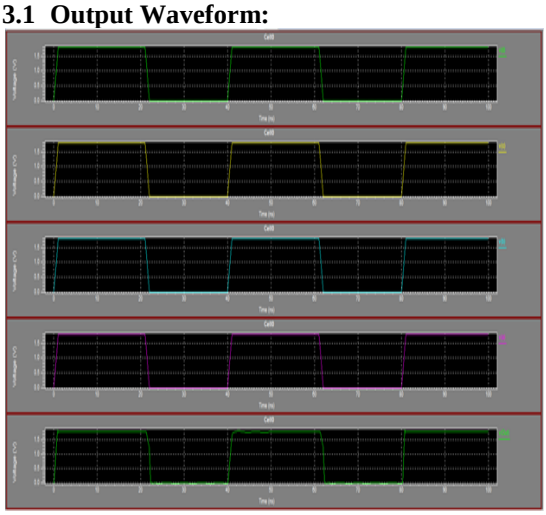

Fig 10: Output waveform of OR gate

IV. IMPLEMENTATION OF 3-BIT FLASH ADC USING THE ABOVE IMPLEMENTED COMPARATOR AND ENCODER (IN TANNER EDA)

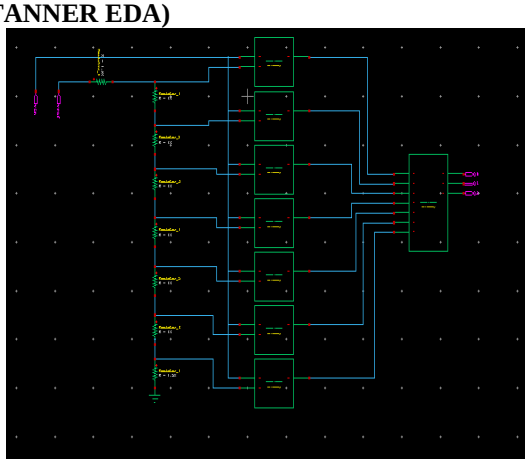

Fig. 11: 3-bitFlash ADC

4.1 Output Waveform:

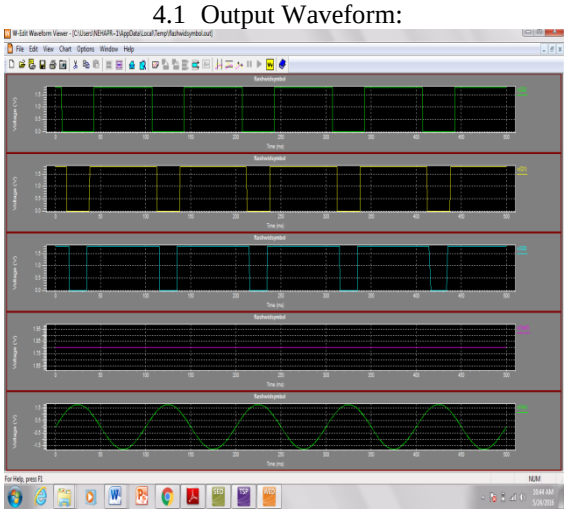

Fig 12: Transient analysis of 3-bit Flash Adcwith MSB and LSB

4.2 Power Results:

VV1 from time 1e-009 to 1e-006
Average power consumed -> 1.947820e-017 watts
Max power 3.891749e-017 at time 1e-006
Min power 3.891749e-020 at time 1e-009

V. CONCLUSION

This paper concludes with the full custom design of a two stage open loop comparator, a priority encoder and finally a Flash ADC.A simple and fast Flash ADC architecture that uses a CMOS open loop comparator has been proposed and an 8 to 3 priority encoder has been used. The encoder has been implemented using 4 inputs OR gates. The results are summarized in the following table. The circuit design and simulation results of 3-bit Flash ADC using 0.18um technology have been presented using TANNER-EDA environment. The power supply voltage given is 1.8v.Though Flash ADC is power hungry andcomplex circuit, so it is a challenge to design and implement low power ADC with high speed applications. Moreover, the architecture of ADC can be extended from medium-to-high resolution applications because of the simplicity of the circuit and also the circuit should be portable to smaller feature size CMOS technologies with lower supply voltages. The result has been summarized in the following table.

Table 3: Specification Summary for Flash ADC

Parameter	Specification
Architecture	Flash
Resolution	3-bit
Power Supply	1.8v
Technology	180nm
Power Dissipation	19.47mw
Area (in terms of transistor count)	79
Frequency	10MHz

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